ELECTRONIC COMPONENTS SUCH AS THIN ARRAY PLASTIC PACKAGES AND PROCESS FOR FABRICATING SAME

CROSS REFERENCE TO RELATED APPLICATION

[0001] This is a continuation-in-part of U.S patent application serial no. 09/802,678 which is a continuation-in-part of of U.S. patent application serial no. 09/288,352, filed April 8, 1999, now U.S. patent no. 6,498,099, which is a continuation-in-part of U.S. patent application serial no. 09/095,803, filed June 10, 1998, now U.S. patent no. 6,229,200.

FIELD OF THE INVENTION

[0002] The present invention relates generally to electronic components and more particularly to a unique construction and process for fabricating electronic components such as thin array plastic packages, inductors and capacitors.

BACKGROUND OF THE INVENTION

[0003] According to well known prior art IC (integrated circuit) packaging methodologies, semiconductor dice are singulated and mounted using epoxy or other conventional means onto respective die attach pads (attach paddles) of a leadframe strip. Traditional QFP (Quad Flat Pack) packages incorporate inner leads which function as lands for wire bonding the semiconductor die bond pads. These inner leads typically require mold locking features to ensure proper positioning of the leadframe strip during subsequent molding to encapsulate the package. The inner leads terminate in outer leads that are bent down to contact a mother board, thereby limiting the packaging density of such prior art devices.

[0004] In order to overcome these and other disadvantages of the prior art, the Applicants previously developed a Leadless Plastic Chip Carrier (LPCC). According to Applicants' LPCC methodology, a leadframe strip is provided for supporting several hundred devices. Singulated IC dice are placed on the strip die attach pads using conventional die mount and epoxy techniques. After curing of the epoxy, the dice are wire bonded to the peripheral internal leads by gold (Au), copper (Cu), aluminum (Al) or doped aluminum wire bonding. The leadframe strip is then molded in plastic or resin using a modified mold wherein the bottom cavity is a flat plate.

In the resulting molded package, the die pad and leadframe inner leads are exposed. By exposing the bottom of the die attach pad, mold delamination at the bottom of the die pad is eliminated, thereby increasing the moisture sensitivity performance. Also, thermal performance of the IC package is improved by providing a direct thermal path from the exposed die attach pad to the motherboard. By exposing the leadframe inner leads, the requirement for mold locking features is eliminated and no external lead standoff is necessary, thereby increasing device density and reducing package thickness over prior art methodologies. The exposed inner leadframe leads function as solder pads for motherboard assembly such that less gold wire bonding is required as compared to prior art methodologies, thereby improving electrical performance in terms of board level parasitics and enhancing package design flexibility over prior art packages (i.e. custom trim tools and form tools are not required). These and several other advantages of Applicants' own prior art LPCC process are discussed in Applicants' United States patent no. 6,229,200, the contents of which are incorporated herein by reference.

[0005] According to Applicants' U.S. patent no. 6,498,099, the contents of which are incorporated herein by reference, an etch back process is provided for the improved manufacture of the LPCC IC package. In Applicant's co-pending U.S. application serial no. 09/802,678, Entitled Leadless Plastic Chip Carrier With Etch Back Pad Singulation, filed March 9, 2001, the contents of which are incorporated herein by reference, the etch-back LPCC process of Applicants' United States patent no. 6,498,099 is modified to provide additional design features. The leadframe strip is selectively covered with a thin layer photo-resist mask in predetermined areas. Following the application of the mask, an etch-barrier is deposited as the first layer of the contact pads and die attach pad, followed by several layers of metals which can include for example, Ni, Cu, Ni, Au, and Ag. This method of formation of the contact pads allows plating of the pads in a columnar shape and into a "mushroom cap" or rivet-shape as it flows over the photoresist mask. The shaped contact pads are thereby locked in the mold body, providing superior board mount reliability. Similarly, the die attach pad can be formed in an interlocking shape for improved alignment with the die. The photo-resist mask is then rinsed away and the semiconductor die is mounted to the die attach pad. This is followed by gold wire bonding between the semiconductor die and the peripheral contact pads and then molding as described in Applicant's United States patent no. 6,229,200. The leadframe is then subjected to full immersion in an alkaline etchant that exposes a lower surface of an array of the contact pads, a power ring and the die attach pad, followed by singulation of the individual unit from the full leadframe array strip. This process includes the deposition or plating of a plurality of layers

of metal to form a robust three-dimensional construction of contact pads and the die attach pad.

[0006] Still further improvements in high performance integrated circuit (IC) packages are driven by industry demands for increased thermal and electrical performance, decreased size and cost of manufacture. For particular applications, demand exists for multi-functional high performance packages with integrated electronic components.

[0007] It is therefore desirable to provide a process for fabricating electronic components such as thin array plastic packages including inductors and capacitors.

SUMMARY OF THE INVENTION

[0008] In one aspect of the present invention, there is provided process for fabricating an integrated circuit package includes establishing a plating mask on a first surface of a metal carrier, the plating mask defining a plurality of components including at least one die attach pad, at least one row of contact pads and at least one additional electronic component. A plurality of metallic layers are deposited on exposed portions of the first surface of the metal carrier, thereby forming the plurality of components. The plating mask is stripped from the metal carrier and leaving the plurality of metallic layers in the form of the plurality of components. At least one semiconductor die is mounted to a respective one of the at least one die attach pad such that each die attach pad has a respective semiconductor die mounted thereon and pads of each the respective semiconductor die are electrically connected to ones of the contact pads and to the additional electronic component. The first surface of the metal carrier is overmolded to encapsulate the plurality of components and the at least one semiconductor die and the metal carrier is etched away.

[0009] In another aspect of the present invention, there is provided an integrated circuit package having a plurality of components including at least one die attach pad, at least one row of contact pads and at least one additional electronic component, the plurality of components comprising a plurality of metallic layers. At least one semiconductor die is mounted to a respective one of the at least one die attach pad and electrically connected to the ones of the contact pads and to the additional electronic component. An overmold covers the at least one semiconductor die and the plurality of components.

[0010] In yet another aspect of the present invention, there is provided a process for

fabricating an electronic component including establishing a suitable plating mask for the desired electronic component, on a first surface of a metal carrier. A plurality of metallic layers are deposited on exposed portions of the first surface of the metal carrier. The plating mask is stripped from the metal carrier to thereby leave the plurality of metallic layers in the form of the electronic component.

[0011] Advantageously, the thin array plastic package includes electronic components within the package. The process of an aspect of the present invention provides for the fabrication of thin array plastic packages including inductors and capacitors using a selective plating process. In another aspect of the present invention, a similar plating process is employed in manufacturing individual inductors and capacitors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The invention will be better understood with reference to the drawings and the following description, in which:

[0013] Figures 1A to 1J show process steps for fabricating an integrated circuit package, in accordance with one embodiment of the present invention;

[0014] Figures 2A to 2J show process steps for fabricating an integrated circuit package, in accordance with another embodiment of the present invention;

[0015] Figures 3A to 3J show process steps for fabricating another integrated circuit package, in accordance with still another embodiment of the present invention;

[0016] Figures 4A to 4E show process steps for fabricating a capacitor, in accordance with yet another embodiment of the present invention;

[0017] Figures 5A to 5D show process steps for fabricating an inductor, in accordance with another embodiment of the present invention;

[0018] Figure 6(1) shows a top view of an alternative embodiment of the integrated circuit package 20 of the present invention;

[0019] Figure 6(2) shows a sectional side view taken along the line 2-2 of Figure 6(1);

[0020] Figure 7(1) shows a top view of an alternative embodiment of the integrated circuit package 20 of the present invention; and

[0021] Figure 7(2) shows a sectional side view taken along the line 2-2 of Figure 7(1).

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] Reference is made to Figures 1A to 1K to describe processing steps for fabricating an integrated circuit package according to a first embodiment of the present invention, indicated generally by the numeral 20. The integrated circuit package 20 has a plurality of components including at least one die attach pad 22, at least one row of contact pads 24 and at least one additional electronic component. The plurality of components are comprised of a plurality of metallic layers. At least one semiconductor die 26 is mounted to a respective one of the at least one die attach pad 22 and electrically connected to the ones of the contact pads 24 and to the at least one additional electronic component. An overmold 28 covers the at least one semiconductor die 26 and the plurality of components.

[0023] The processing steps for fabricating the integrated circuit (IC) package 20 will now be described with reference to Figures 1A to 1K. Reference is first made to Figure 1A(1), which shows a top view of a metal strip 30, and to Figure 1A(2), which shows a side view of the metal strip 30. The metal strip 30 acts as a carrier on which the IC package 20 is fabricated. It will be understood that in the present embodiment, the metal strip 30 is a copper strip that does not form part of the IC package 20 shown in Figure 1K(1) and 1K(2). The metal strip 30 is not limited to copper, however, as other metals are possible. The metal strip 30 is large for the fabrication of several IC packages on the single metal strip 30. Thus, the IC package of the present embodiment is gang fabricated. Only one such package is shown formed on the strip 30 in the following Figures, portions of adjacent packages are shown by stippled lines. For the purpose of simplicity, however, reference is made only to the single IC package in the following description.

[0024] A plating mask 32 is then established on one surface of the metal strip 30, as shown in Figures 1B(1) and 1B(2), which show a top view and a sectional side view along the line 2-2 of Figure 1B(1), respectively, of the metal strip 30 including the plating mask 32. To establish the plating mask 32 as shown in the Figures, the metal strip 30 is coated with a layer of photo-imageable plating mask such as photo-imageable epoxy. Next, the layer of photo-imageable plating mask is imaged with a photo-tool. This is accomplished by exposure of the photo-imageable plating mask to ultraviolet light masked by the photo-tool and subsequent developing

of the plating mask, as will be understood by those skilled in the art. The plating mask is thereby patterned to provide pits in which the upper surface of the metal strip is exposed. It will be appreciated that the plating mask 32 is thereby established and this plating mask 32 defines the plurality of components that are added in the following steps. In the present embodiment, the plating mask 32 defines the two die attach pads 22, the contact pads 24, an inductor 34 and a capacitor 36.

[0025] Next, several layers of metal are deposited on the upper surface of the exposed metal strip 30 to form the die attach pads 22, the contact pads 24, the inductor 34 and the capacitor 36. Figures 1C(1) and 1C(2) show a top view and a sectional side view taken along the line 2 – 2 of Figure 1C(1), respectively, of the metal strip 30 with the deposited metal layers. Different deposition options are available. According to plating option 1, shown in Figure 1C(3), a layer of flash Cu (for example 25 microinches) is provided over the Cu substrate for creating an etch down cavity following post etching, as will be described below. An etch barrier of gold (Au) of, for example, 20 microinches is then deposited, followed by layers of nickel (Ni) of 40 microinches, copper (Cu) of 3 to 4 mils, nickel (Ni) of 40 microinches, and gold (Au) of 20 microinches. It will be appreciated that the thicknesses of the deposited metal layers are given for exemplary purposes.

[0026] In plating option 2, an initial layer of flash Cu is deposited on the copper substrate, followed by an etch barrier of palladium (Pd), followed by layers of Ni, Cu, Ni, and Pd, as shown in Figure 1C(4).

[0027] In plating option 3, an initial layer of flash Cu is deposited on the copper substrate, followed by an etch barrier of Ag, followed by layers of Cu and Ag, as shown in Figure 1C(5).

[0028] In plating option 4, an initial layer of flash Cu is deposited on the copper substrate, followed by an etch barrier of Pd, followed by Ni and Pd, as shown in Figure 1C(6).

[0029] In plating option 5, an initial layer of Cu is deposited on the copper substrate, followed by Ag, as shown in Figure 1C(7).

[0030] After plating, the plating mask 32 is stripped away by conventional means resulting in the metal strip 30 with the die attach pads 22, contact pads 24, inductor 34 and capacitor 36 formed thereon. The metal strip 30 and the components with the plating mask 32 stripped away are shown in Figures 1D(1) and 1D(2), which show a top view and a sectional side view along the line 2-2 of Figure 1D(1), respectively, of the metal strip 30 and components without the

plating mask 32.

[0031] As shown in Figures 1E(1) and 1E(2), which show a top view and a sectional side view along the line 2-2 of Figure 1E(1), respectively, each singulated semiconductor die 26 of a total of two semiconductor dice 26, is mounted to a respective die attach pad 22, using known techniques. In the present embodiment, the semiconductor dice are attached using silver-filled epoxy, as will be understood by those skilled in the art. In an alternative embodiment, solder paste is dispensed on each die attach pad 22 and each respective semiconductor die 26 is attached by a solder reflow technique. In this alternative embodiment, the semiconductor dice 32 are coated with a suitable surface for soldering, such as titanium (Ti), tungsten (W) or gold (Au) for mounting by solder reflow technique.

[0032] After mounting the semiconductor dice 26, wires 38 are bonded between pads of the semiconductor dice 26 and ones of the contact pads 24. Wires 38 are also bonded between the pads of the semiconductor dice 26 and the inductor 34 and between pads of the semiconductor dice 26 and the capacitor 36. Thus, the semiconductor dice 26 are mounted and are electrically connected to ones of the contact pads 24, the inductor 34 and the capacitor 36. The wires 38 are made of a suitable wire-bonding material such as Au, Cu, aluminum (Al) or doped aluminum.

[0033] Overmolding follows to encapsulate the components, the semiconductor dice 26 and the wires 38, as shown in Figures 1F(1) and 1F(2), which show a top view and a sectional side view taken along the line 2-2 of Figure 1F(1), respectively. To overmold, the metal strip 30, including the components, the semiconductor dice 26 and wires 38, is placed in a mold with a flat plate bottom, molded in an overmold material 28 and cured.

[0034] Next, the metal strip 30 is etched away by subjecting the metal strip 30 to an alkaline etch using a full immersion etch. In the present embodiment, the metal strip 30 is copper and the first layer of metal deposited in forming the components was also copper (flash Cu). The alkaline etch etches away the metal strip 30 and the first layer of metal of the die attach pads 24, the contact pads 26, the inductor 34 and the capacitor 36. Thus, an etch down cavity is formed at each of the components and the die attach pads 22, the contact pads 24, the inductor 34 and the capacitor 36 are exposed. The resulting package is shown in Figures 1G(1) and 1G(2), which show a bottom view and a sectional side view taken along line 2-2 of Figure 1G(1), respectively.

[0035] A solder mask 40 is then formed in selected areas of the etch down cavities, resulting in the pattern shown in Figures 1H(1) and 1H(2) which show a bottom view and a sectional side view taken along line 2-2 of Figure 1H(1). The solder mask 40 is formed in selected areas by solder mask printing to cover passive components including the inductor 34 and the capacitor 36. Also, portions of the die attach pads 22 are covered, as shown, leaving the contact pads 24 and portions of the die attach pads 22 exposed.

[0036] Solder balls 42 are then fixed to the exposed contact pads 24 and the exposed portions of the die attach pads 22, as shown in Figure 1I, which shows a sectional side view of the resulting package. To attach the solder balls 42, a flux is first added to the solder balls 42 and, after placement in position in the etch down cavities that remain after forming the solder mask 40, the solder balls 40 are reflowed using known reflow techniques. The solder balls 42 thus provide electrical connections from the semiconductor dice 26, through the wires 38 and the contact pads 24 and from the die attach pads 22. Excess flux is removed by cleaning with a suitable cleaner.

[0037] The etch down cavities provide good shear strength of solder balls 42 fixed within the etch down cavities. Also, the solder mask 40 under the inductor 34, the capacitor 36 and portions of the die attach pad 22 is better retained because of the etch down cavity formed, thereby protecting these components from the environment.

[0038] Singulation of the individual integrated circuit package 20 from the remaining packages is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 1J.

[0039] Reference is now made to Figures 2A to 2J to describe the processing steps for fabricating an integrated circuit package 20 according to another embodiment of the present invention. Many of the steps for fabricating the integrated circuit package 20 of Figures 2A to 2J are similar to the steps for fabricating the integrated circuit package 20 of Figures 1A to 1J described above.

[0040] Similar to Figures 1A(1) and 1A(2), Figure 2A(1), shows a top view of the metal strip 30, and Figure 2A(2) shows a side view of the metal strip 30. The metal strip 30 of the present embodiment is similar to the metal strip 30 previously described and therefore is not further described herein.

[0041] A plating mask 32 is then established on one surface of the metal strip 30, as shown

in Figures 2B(1) and 2B(2), which show a top view and a sectional side view along the line 2-2 of Figure 2B(1), respectively, of the metal strip 30 including the plating mask 32. The plating mask 32 is established in the same manner that the plating mask 32 is established in the first described embodiment. In the present embodiment, however, the plating mask 32 defines a single die attach pad 22, the contact pads 24, an inductor 34, a capacitor 36 and a circuit pattern in the form of circuit traces 44 that extend from each of the contact pads 24, and end proximal the die attach pad 22.

[0042] Next, several layers of metal are deposited on the upper surface of the exposed metal strip 30 to form the die attach pad 22, the contact pads 24, the inductor 34, the capacitor 36 and the circuit traces 44. Figures 2C(1) and 2C(2) show a top view and a sectional side view taken along the line 2 – 2 of Figure 2C(1), respectively, of the metal strip 30 with the deposited metal layers. The plating options in the present embodiment are similar to those of the first described embodiment and are shown in Figures 2C(3) to 2C(7).

[0043] After plating, the plating mask 32 is stripped away by conventional means resulting in the metal strip 30 with the die attach pad 22, contact pads 24, inductor 34, capacitor 36 and circuit traces 44 formed thereon. The metal strip 30 and the components with the plating mask 32 stripped away are shown in Figures 2D(1) and 2D(2), which show a top view and a sectional side view along the line 2-2 of Figure 1D(1), respectively, of the metal strip 30 without the plating mask 32.

[0044] A singulated semiconductor die 26 is mounted to the die attach pad 22, using known techniques, as shown in Figures 2E(1) and 2E(2) which show a top view and a sectional side view along the line 2-2 of Figure 2E(1), respectively.

[0045] After mounting the semiconductor die 26, wires 38 are bonded between pads of the semiconductor die 26 and the circuit traces 44 that extend inwardly toward the die attach pad 22. Wires 38 are also bonded between the pads of the semiconductor die 26 and the inductor 34 and between pads of the semiconductor die 26 and the capacitor 36. Thus, the semiconductor die 26 is mounted and is electrically connected to the contact pads 24 through the circuit traces 44 and the wires 38, and is electrically connected to the inductor 34 and the capacitor 36 through wires 38.

[0046] Overmolding in an overmold material 28 follows, as shown in Figures 2F(1) and 2F(2), which show a top view and a sectional side view taken along the line 2-2 of Figure 2F(1),

respectively.

[0047] Next, the metal strip 30 is etched away by subjecting the metal strip 30 to an alkaline etch using a full immersion etch, leaving etch down cavities at each of the die attach pad 22, the contact pads 24, the inductor 34, the capacitor 36 and the circuit traces 44. The resulting package is shown in Figures 2G(1) and 2G(2), which show a bottom view and a sectional side view taken along line 2-2 of Figure 2G(1), respectively.

[0048] A solder mask 40 is then formed in selected areas of the etch down cavities, resulting in the pattern shown in Figures 2H(1) and 2H(2) which show a bottom view and a sectional side view taken along line 2-2 of Figure 2H(1), respectively. The solder mask 40 is formed in selected areas by solder mask printing to cover passive components including the inductor 34 and the capacitor 36. Also, the circuit traces 44 and portions of the die attach pad 22 are covered, as shown, leaving the contact pads 24 and portions of the die attach pad 22 exposed.

[0049] Solder balls 42 are then fixed to the exposed contact pads 24 and the exposed portions of the die attach pad 22, as shown in Figure 2I, which shows a sectional side view of the resulting package. Again, the etch down cavities provide good shear strength of solder balls 42 fixed within the etch down cavities. Also, the solder mask 40 under the inductor 34, the capacitor 36 and portions of the die attach pad 22 is better retained because of the etch down cavity formed, thereby protecting these components from the environment.

[0050] Singulation of the individual integrated circuit package 20 from the remaining packages is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 2J.

[0051] Reference is now made to Figures 3A to 3J to describe the processing steps for fabricating an integrated circuit package 20 according to still another embodiment of the present invention. Many of the steps for fabricating the integrated circuit package 20 of Figures 3A to 3J are similar to the steps for fabricating the integrated circuit package 20 of Figures 2A to 2J described above.

[0052] Similar to Figures 2A(1) and 2A(2), Figure 3A(1), shows a top view of the metal strip 30, and Figure 3A(2) shows a side view of the metal strip 30. The metal strip 30 of the present embodiment is similar to the metal strip 30 previously described and therefore is not further described herein.

[0053] A plating mask 32 is then established on one surface of the metal strip 30, as shown in Figures 3B(1) and 3B(2), which show a top view and a sectional side view along the line 2-2 of Figure 3B(1), respectively, of the metal strip 30 including the plating mask 32. The plating mask 32 is established in the same manner that the plating mask 32 is established in the first described embodiment. In the present embodiment, however, the plating mask 32 defines a single die attach pad 22, the contact pads 24, an inductor 34, a capacitor 36 and a circuit pattern in the form of circuit traces 44 that extend from each of the contact pads 24, and end proximal the die attach pad 22. Additional circuit traces 46 also extend from the inductor 34 to an end proximal the die attach pad 22 and from the capacitor 36 to an end proximal the die attach pad 22.

[0054] Next, several layers of metal are deposited on the upper surface of the exposed metal strip 30 to form the die attach pad 22, the contact pads 24, the inductor 34, the capacitor 36, the circuit traces 44 and the circuit traces 46. Figures 3C(1) and 3C(2) show a top view and a sectional side view taken along the line 2 – 2 of Figure 3C(1), respectively, of the metal strip 30 with the deposited metal layers. The plating options in the present embodiment are similar to those of the first described embodiment. However, in the present embodiment, an additional masking process is carried out to provide contacts for mounting the flip-chip semiconductor die. for example, in the case of plating option 1, the first four layers of Cu, Au, Ni and Cu are deposited. Next, a second plating mask 48 is added to define contacts 49 on the die attach pad 22, the circuit traces 44 and the circuit traces 46. The remaining two metal layers of Ni and Au are then deposited to form contacts 49.

[0055] After plating, the plating mask 32 is stripped away by conventional means resulting in the metal strip 30 with the die attach pad 22, contact pads 24, inductor 34, capacitor 36, circuit traces 44 and circuit traces 46 formed thereon. The metal strip 30 and the components with the plating mask 32 stripped away are shown in Figures 3D(1) and 3D(2), which show a top view and a sectional side view along the line 2-2 of Figure 2D(1), respectively, of the metal strip 30 without the plating mask 32. Clearly the contacts 49 protrude from the remainder of the deposited metal layers of the die attach pad 22, the circuit traces 44 and the circuit traces 46.

[0056] Reference is now made to Figures 3E(1) and 3E(2) which show a top view and a sectional side view along the line 2-2 of Figure 3E(1), respectively. As shown, a singulated semiconductor die 26 is mounted to the die attach pad 22, in a flip-chip orientation, using known techniques. In this orientation, the semiconductor die 26 is attached to the contacts 49 of the

die attach pad 22, the circuit traces 44 and the circuit traces 46 by direct solder attach of pads of the semiconductor die 30 to the contacts 49. Thus, the pads of the semiconductor die 30 are electrically connected to the die attach pad 22, the circuit traces 44 and the circuit traces 46.

[0057] Overmolding in an overmold material 28 follows, as shown in Figures 3F(1) and 3F(2), which show a top view and a sectional side view taken along the line 2-2 of Figure 3F(1), respectively.

[0058] Next, the metal strip 30 is etched away by subjecting the metal strip 30 to an alkaline etch using a full immersion etch, leaving etch down cavities at each of the die attach pad 22, the contact pads 24, the inductor 34, the capacitor 36, the circuit traces 44 and the circuit traces 46. The resulting package is shown in Figures 3G(1) and 3G(2), which show a bottom view and a sectional side view taken along line 2-2 of Figure 3G(1), respectively.

[0059] A solder mask 40 is then formed in selected areas of the etch down cavities, resulting in the pattern shown in Figures 3H(1) and 3H(2) which show a bottom view and a sectional side view taken along line 2-2 of Figure 3H(1), respectively. The solder mask 40 is formed in selected areas by solder mask printing to cover passive components including the inductor 34 and the capacitor 36. Also, the circuit traces 44, the circuit traces 46, and portions of the die attach pad 22 are covered, as shown, leaving the contact pads 24 and portions of the die attach pad 22 exposed.

[0060] Solder balls 42 are then fixed to the exposed contact pads 24 and the exposed portions of the die attach pad 22, as shown in Figure 3I, which shows a sectional side view of the resulting package.

[0061] Singulation of the individual integrated circuit package 20 from the remaining packages is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 3J.

[0062] Reference is now made to Figures 4A to 4E to describe the process steps for fabricating a capacitor 36, in accordance with yet another embodiment of the present invention. Some of the steps for fabricating the capacitor 36 of Figures 4A to 4E are similar to the steps for fabricating the integrated circuit package 20 of Figures 1A to 1J described above.

[0063] Similar to Figures 1A(1) and 1A(2), Figure 4A(1), shows a top view of the metal strip 30, and Figure 4A(2) shows a side view of the metal strip 30. The metal strip 30 of the present embodiment is similar to the metal strip 30 previously described and therefore is not further

described herein.

[0064] A plating mask 32 is then established on one surface of the metal strip 30, as shown in Figures 4B(1), 4B(2), and 4B(3), which show a top view, a sectional side view taken along the line 2-2, and a sectional side view taken along the line 3-3 of Figure 4B(1), respectively, of the metal strip 30 including the plating mask 32. The plating mask 32 is established in the same manner that the plating mask 32 is established in the first described embodiment. In the present embodiment, however, the plating mask 32 defines the capacitor 36 only.

[0065] Next, several layers of metal are deposited on the upper surface of the exposed metal strip 30 to form the capacitor 36. Figures 4C(1), 4C(2), and 4C(3) show a top view, a sectional side view taken along the line 2 – 2 and a sectional side view taken along the line 3-3 of Figure 4C(1), respectively, of the metal strip 30 with the deposited metal layers. The plating options in the present embodiment are similar to those of the first described embodiment and therefore are not further described herein.

[0066] After plating, the plating mask 32 is stripped away by conventional means resulting in the metal strip 30 with the capacitor 36 formed thereon. The metal strip 30 and the capacitor 36 with the plating mask 32 stripped away are shown in Figures 4D(1), 4D(2) and 4D(3), which show a top view, a sectional side view taken along the line 2-2 and a sectional side view taken along the line 3-3 of Figure 4D(1), respectively of the metal strip 30 including the capacitor 36 with the plating mask 32 stripped away.

[0067] Next, a dielectric material 50 is selectively deposited between plates of the capacitor 36, as shown in Figures 4E(1), 4E(2) and 4E(3), which show a top view, a sectional side view taken along the line 2-2 and a sectional side view taken along the line 3-3 of Figure 4E(1), respectively of the metal strip 30 including the capacitor 36 with the dielectric material 50 disposed between the plates of the capacitor 36. In the present embodiment, the dielectric material 50 is an electrically non-conductive epoxy that is selectively screen printed between the plates of the capacitor 36. Other dielectric materials are possible, however.

[0068] Reference is now made to Figures 5A to 5D to describe the process steps for fabricating an inductor 34, in accordance with still another embodiment of the present invention. Some of the steps for fabricating the inductor 34 of Figures 5A to 5D are similar to the steps for fabricating the capactor 36 of Figures 4A to 4E described above.

[0069] Similar to Figures 4A(1) and 4A(2), Figure 5A(1), shows a top view of the metal strip

30, and Figure 5A(2) shows a side view of the metal strip 30. The metal strip 30 of the present embodiment is similar to the metal strip 30 previously described and therefore is not further described herein.

[0070] A plating mask 32 is then established on one surface of the metal strip 30, as shown in Figures 5B(1) and 5B(2), which show a top view and a sectional side view taken along the line 2-2 of Figure 5B(1), respectively, of the metal strip 30 including the plating mask 32. The plating mask 32 is established in the same manner that the plating mask 32 is established in the above described embodiments. In the present embodiment, however, the plating mask 32 defines the inductor 34 only.

[0071] Next, several layers of metal are deposited on the upper surface of the exposed metal strip 30 to form the inductor 34. Figures 5C(1) and 5C(2) show a top view and a sectional side view taken along the line 2 – 2 of Figure 5C(1), respectively, of the metal strip 30 with the deposited metal layers. The plating options in the present embodiment are similar to those of the above described embodiments and therefore are not further described herein.

[0072] After plating, the plating mask 32 is stripped away by conventional means resulting in the metal strip 30 with the inductor 34 formed thereon. The metal strip 30 and the inductor 34 with the plating mask 32 stripped away are shown in Figures 5D(1) and 5D(2), which show a top view and a sectional side view taken along the line 2-2 of Figure 5D(1), respectively, of the metal strip 30 including the inductor 34 with the plating mask 32 stripped away.

[0073] Alternative embodiments of the present invention are possible. For example, rather than simply plating up metal layer after metal layer in the first described embodiment, one or more additional masking processes can be carried out to provide different plating features such as a depression in the die attach pad 22 in which the semiconductor die 26 is mounted. Also, an L-shaped plating feature on the die attach pad 22 providing a depression in which the semiconductor die 26 is mounted, is possible. These features are shown in Figure 6(1) which shows a top view of integrated circuit package 20 after plating of the metal layers and prior to stripping the plating mask, according to an alternative embodiment of the present invention, and Figure 6(2) which shows a sectional side view taken along the line 2-2 of Figure 6(1). Similarly, an alternative to the second described embodiment is shown in Figure 7(1) which shows a top view of an integrated circuit package 20 after plating of the metal layers and prior to stripping the plating mask, according to another alternative embodiment of the present invention, and Figure 7(2) which shows a sectional side view taken along the line 2-2 of Figure 7(1). In this

embodiment, additional masking processes are carried out between deposition of the layers of metal, resulting in the semiconductor package 20 with a depression in the die attach pad 22 and depressed circuit traces 44, as shown. The fourth and fifth described embodiments can also be modified as additional masking processes can be carried out to provide different plating features on the capacitor and the inductor, respectively.

[0074] Other modifications and variations to the above-described embodiments are possible. For example, the plating options described above are provided for exemplary purposes and other alternative plating options are also possible. Also, the dielectric material disposed between the plates of the capacitor in the embodiment of Figures 4A to 4F is not limited to an electrically non-conductive epoxy as other dielectric materials can be used. For example, a molding compound can be used as the dielectric material. Still other modifications and variations may occur to those skilled in the art. It is intended that all such modifications and variations fall within the true spirit and scope of the present invention.